CLAIMS:

1. A return-to-zero (RZ) recovery system comprising:

filter configured to receive a data signal and to reduce high frequency components from the data signal to form a filtered data signal;

recovery unit configured to receive the filtered data signal identify a first type of data transition and provide phase information when the first type of data transition is identified.

2. The system of claim 1 wherein the first type of data transition is a logical one to a logical zero transition.

3. The system of claim 1 wherein the first type of data transition is a logical zero to a logical one transition.

4. The system of claim 1 wherein the filter is a low pass filter.

5. The system of claim 4 wherein the data signal is a RZ data signal and the filter is further configured to convert the RZ data signal into a non-return-to-zero (NRZ) data signal.

6. The system of claim 1 wherein the filter qualifies that a logical one is valid when a specific voltage level is maintained for a specific amount of time.

7. The system of claim 1 wherein the recovery unit adjusts the data signal based on the occurrence of the first and second data transitions.

8. The system of claim 1 wherein the recovery unit comprises phase detector determining phase difference between a recovered clock signal and the data signal.

9. The system of claim 8 wherein the phase detector generates a phase difference signal based on the determined phase difference.

10. The system of claim 9 wherein the phase difference signal is proportional to determined phase difference.

11. The system of claim 8 wherein the recovery unit further comprises an inhibitor receiving a phase difference signal and the data signal, the inhibitor determining if the first type of data transition has occurred.

12. The system of claim 11 wherein the recovery unit further comprises loop filter receiving the phase difference signal from the inhibitor if the first type of data transition has occurred.

13. The system of claim 12 wherein the recovery unit further comprises a oscillator and wherein the loop filter filters the phase difference signal and provides the filtered phase difference signal to the oscillator.

14. The system of claim 13 wherein the filtered phase difference signal acts as a control voltage to the oscillator.

15. The system of claim 13 wherein the oscillator

generates the recovered clock signal based on the filtered phase difference signal.

16. The system of claim 13 wherein the oscillator adjusts the frequency of the recovered clock signal based on the filtered phase difference signal.

17. The system of claim 1 wherein the recovery unit comprises phase detector determining a phase difference between a recovered clock signal and the data signal when the first type of data transition has occurred.

18. The system of claim 17 wherein the phase detector determines if the first type of data transition has occurred.

19. The system of claim 1 wherein the recovery unit comprises inhibitor receiving the data signal and determines if the first type of data transition occurs.

20. The system of claim 19 wherein the recovery unit comprises a phase detector and wherein the inhibitor provides the data signal to the phase detector when the first type of data transition occurs.

21. A method of sampling return-to-zero data, the method comprising:

receiving a data signal;

identifying a transition to a second data state from a first data state; and

providing phase information when the transition is identified.

22. The method of claim 21 wherein the data signal is a return-to-zero data signal.

23. The method of claim 22 further comprising converting the return-to-zero data signal to a non-return-to-zero data signal.

24. The method of claim 23 further comprising removing high frequency components on the return-to-zero data signal.

25. The method of claim 24 further comprising:

identifying a second transition to the first data state from the second data state; and

providing phase information when the second transition is identified.

26. The method of claim 25 further comprising generating a clock signal based on the provided phase information.

27. The method of claim 26 wherein the transition is a rising edge data transition.

28. The method of claim 26 wherein the second transition is a falling edge data transition.

29. A method of sampling return-to-zero data, the method comprising:

determining first phase information from a data signal when a first type of data transition occurs;

determining second phase information from a data signal

when a second type of data transition occurs;

generating a first clock signal based on the first phase information;

generating a second clock signal based on the second phase information; and

generating a third clock signal based on the first and second clock signals.

30. The method of claim 29 further comprising sampling the data signal based on the third clock signal.

31. The method of claim 30 wherein the data signal being a RZ data signal and converting the data signal to a non-return-to-zero data signal.

32. The method of claim 29 wherein the third clock signal is an interpolation of the first and second clock signals.

33. A return-to-zero (RZ) recovery system comprising:

first recovery unit configured to receive a data signal and identifying a first type of data transition and determining a first phase information when the first type of data transition is identified; and

second recovery unit configured to receive the data signal and identifying a second type of data transition and determining second phase information when the second type of data transition is identified.

34. The system of claim 33 wherein the first recovery unit generates a first recovered clock signal based on the determined first phase information and the second recovery unit generates

a second recovered clock signal based on the determined second phase information.

35. The system of claim 34 further comprising a interpolator generating a third recovered clock signal based on the first recovered clock signal and the second recovered clock signal.

36. The system of claim 35 wherein the third recovered clock signal is an additive result of the first and the second recovered clock signals.

37. The system of claim 35 wherein the third recovered clock signal is an interpolation of the first and second recovered clock signal.

38. The system of claim 35 wherein the data signal is a RZ data signal and the system further comprises a sampling unit and a filter, the filter converting the RZ data signal into a non-return-to-zero (NRZ) data signal and providing the NRZ data signal to the sampling unit.

39. The system of claim 38 wherein the sampling unit samples the data signal using the third recovered clock signal from the interpolator.

40. The system of claim 34 wherein the data signal is a RZ data signal and the system further comprises a sampling unit and a filter, the filter converting the RZ data signal into a non-return-to-zero (NRZ) data signal and providing the NRZ data signal to the first recovery unit.

41. The system of claim 40 wherein the second recovery unit is disabled.

42. The system of claim 33 wherein the first type of data transition is a low voltage to a high voltage transition.

43. The system of claim 33 wherein the second type of data transition is a high voltage to a low voltage transition.

44. The system of claim 33 wherein a high voltage is a voltage that is greater then the low voltage.

45. The system of claim 33 wherein the first type of data transition is a rising edge data transition.

46. The system of claim 33 wherein the second type of data transition is a falling edge data transition.

47. The system of claim 33 wherein the data signal is a RZ data signal and the system further comprises a filter to convert the RZ data signal into a non-return-to-zero (NRZ) data signal and the filter provides the NRZ data signal to one of the first and second recovery units.

48. The system of claim 33 wherein the first recovery unit comprises a first phase detector determining phase difference between a first recovered clock signal and the data signal.

49. The system of claim 48 wherein the phase detector generates a phase difference signal based on the determined

phase difference.

50. The system of claim 49 wherein the phase difference signal is proportional to determined phase difference.

51. The system of claim 49 wherein the first recovery unit further comprises first loop filter receiving the phase difference signal from the first phase detector.

52. The system of claim 49 wherein the first recovery unit further comprises a oscillator and wherein the first loop filter filters the phase difference signal and provides the filtered phase difference signal to the oscillator.

53. The system of claim 52 wherein the oscillator generates the first recovered clock signal based on the filtered phase difference signal.

54. The system of claim 53 wherein the oscillator adjusts the frequency of the first recovered clock signal based on the filtered phase difference signal.

55. The system of claim 33 wherein the second recovery unit comprises a second phase detector determining phase difference between a second recovered clock signal and the data signal.

56. The system of claim 55 wherein the phase detector generates a phase difference signal based on the determined phase difference

57. The system of claim 56 wherein the second recovery unit further comprises second loop filter receiving the phase difference signal from the second phase detector.

58. The system of claim 57 wherein the first recovery unit further comprises an oscillator and wherein the second loop filter filters the phase difference signal and provides the filtered phase difference signal to the oscillator.

59. The system of claim 58 wherein the oscillator generates the second recovered clock signal based on the filtered phase difference signal.

60. The system of claim 58 wherein the oscillator adjusts the frequency of the second recovered clock signal based on the filtered phase difference signal.

61. The system of claim 35 further comprises a sampling unit sampling the data signal using the third recovered clock signal from the interpolator.